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TFT LCD Tentative Specification

MODEL NO.: V320B1 - L05

LCD TV Head Division	
AVP	郭振隆

QRA Dept.	TVHD / PDD		
	DDIII	DDII	DDI
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 0.0	Mar. 01,'06	All	All	Tentative Specification was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V320B1- L05 is a 32" TFT Liquid Crystal Display module with 16-CCFL Backlight unit and 1ch-LVDS interface. This module supports 1366 x 768 WXGA format and can display true 16.7M colors (8-bit colors). The inverter module for backlight is built-in.

1.2 FEATURES

-High brightness (500 nits)

- Ultra-high contrast ratio (1200:1)
- Faster response time (6.5ms)
- High color saturation NTSC 75%
- Ultra wide viewing angle : 176(H)/176(V) (CR>20) with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Color reproduction (nature color)
- Optimized response time for both 50 Frame rate

1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	708.954(H) x 398.592 (V) (32.02" diagonal)	mm	(1)
Bezel Opening Area	714.96 (H) x 404.6 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1366 x R.G.B. x 768	pixel	
Pixel Pitch (Sub Pixel)	0.1730 (H) x 0.5190 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.7M	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Anti-Glare coating (Haze 25%),Hard coating (3H)	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	759	760	761	mm	(1)
	Vertical(V)	449	450	451	mm	(1)
	Depth(D)	36.95	37.95	38.95	mm	To PCB cover
	Depth(D)	46.4	47.4	48.4	mm	To inverter cover
Weight		6300	6500	6700	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

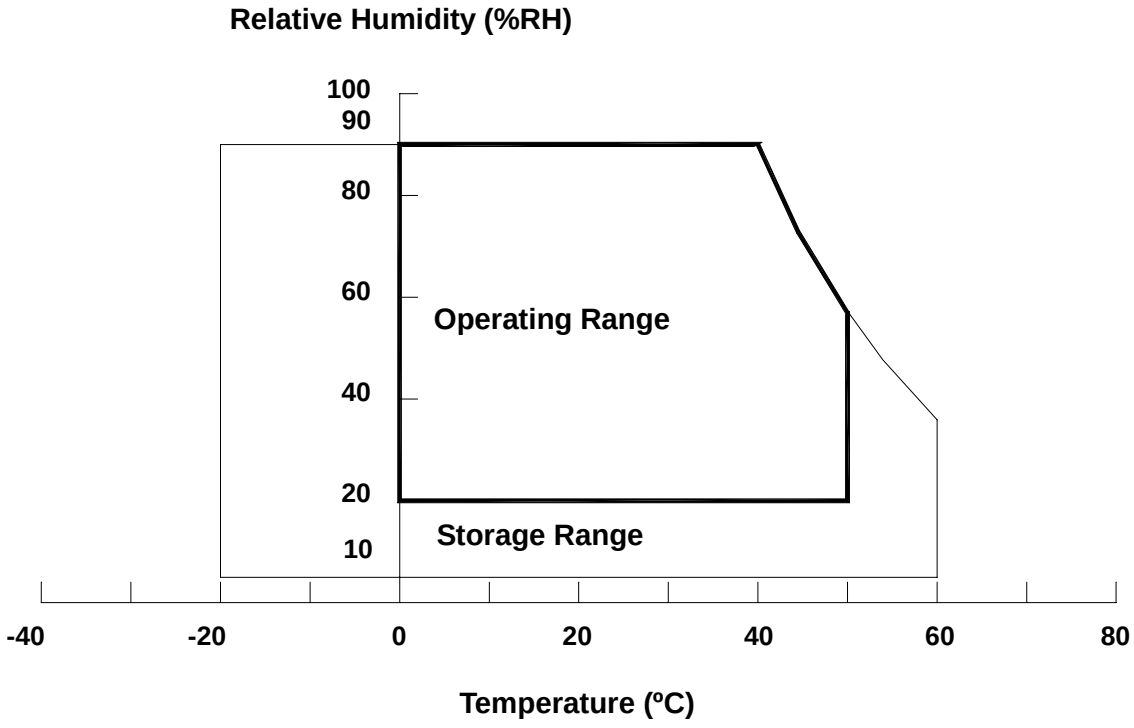
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 60 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.0	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes Backlight On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

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3. ELECTRICAL CHARACTERISTICS

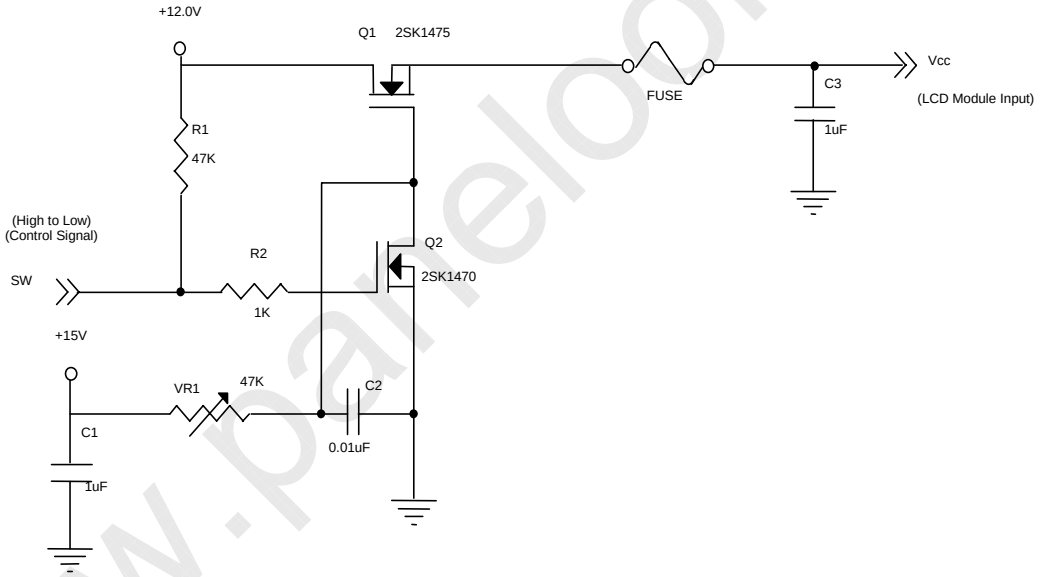
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

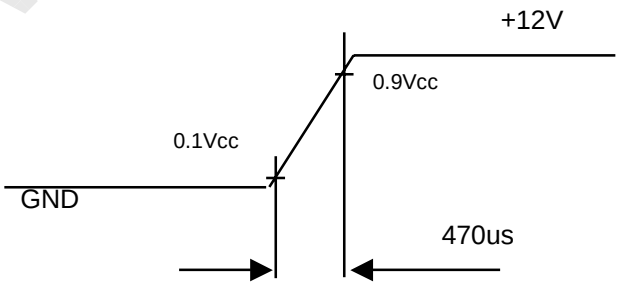
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	11.4	12.0	12.6	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	100	mV	
Rush Current		I_{RUSH}	-	-	2.0	A	(2)
Power Supply Current	White	I_{CC}	-	0.6	0.75	A	(3)
	Black		-	0.3	0.38	A	
	Vertical Stripe		-	0.5	0.65	A	
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	-	-	+100	mV	
	Differential Input Low Threshold Voltage	V_{LVTL}	-100	-	-	mV	
	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



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Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

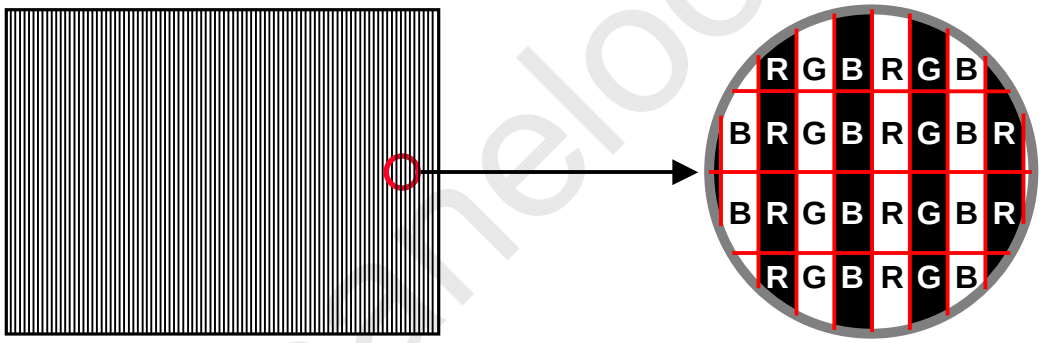
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT INVERTER UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	1285	-	V_{RMS}	I_L = 4.2mA
Lamp Current	I_L	3.7	4.2	4.7	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	2450	V_{RMS}	(2), Ta = 0 ºC
		-	-	2360	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_O	40	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	60,000	-	Hrs	(4)

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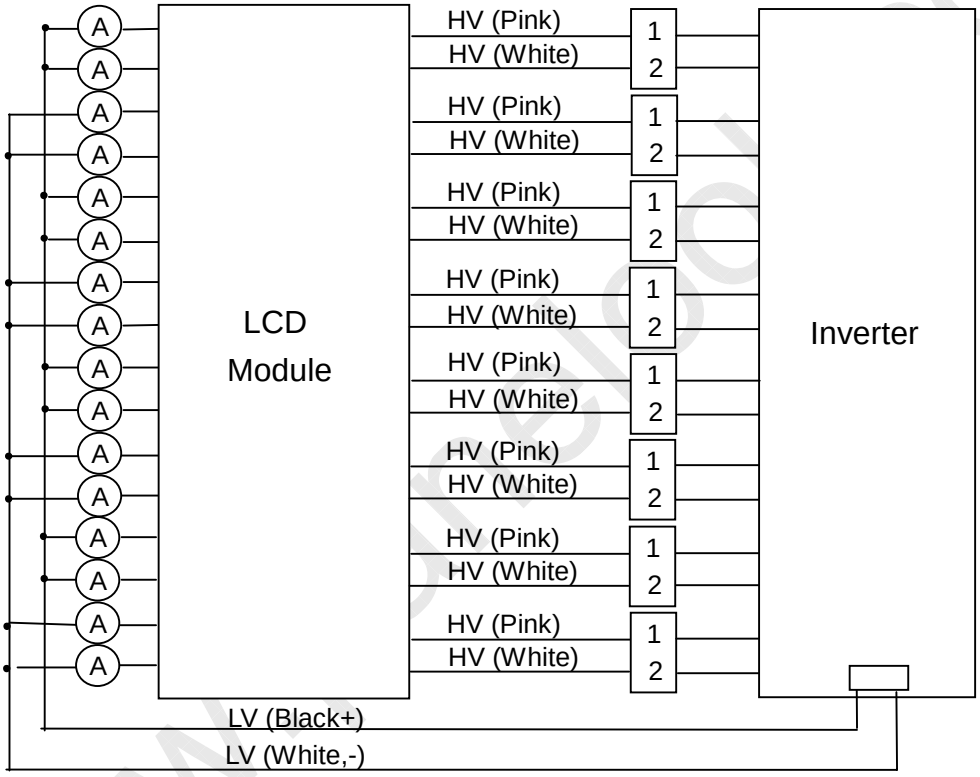
3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	96	104	W	(5),(6), I_L = 6.0mA
Input Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Input Current	I_{BL}	-	4.0	-	A	Non Dimming
Input Ripple Noise	-	-	-	500	mV_{P-P}	V_{BL}=22.8V
Backlight Turn on Voltage	V_{BS}	2450	-	-	V_{RMS}	Ta = 0 ºC
		2360	-	-	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	55	58	61	kHz	
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second under starting up duration. Otherwise the lamp could not be lighted on completed.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the

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condition at Ta = 25 ±2°C and I_L = 3.7 ~ 4.7 mA_{RMS}

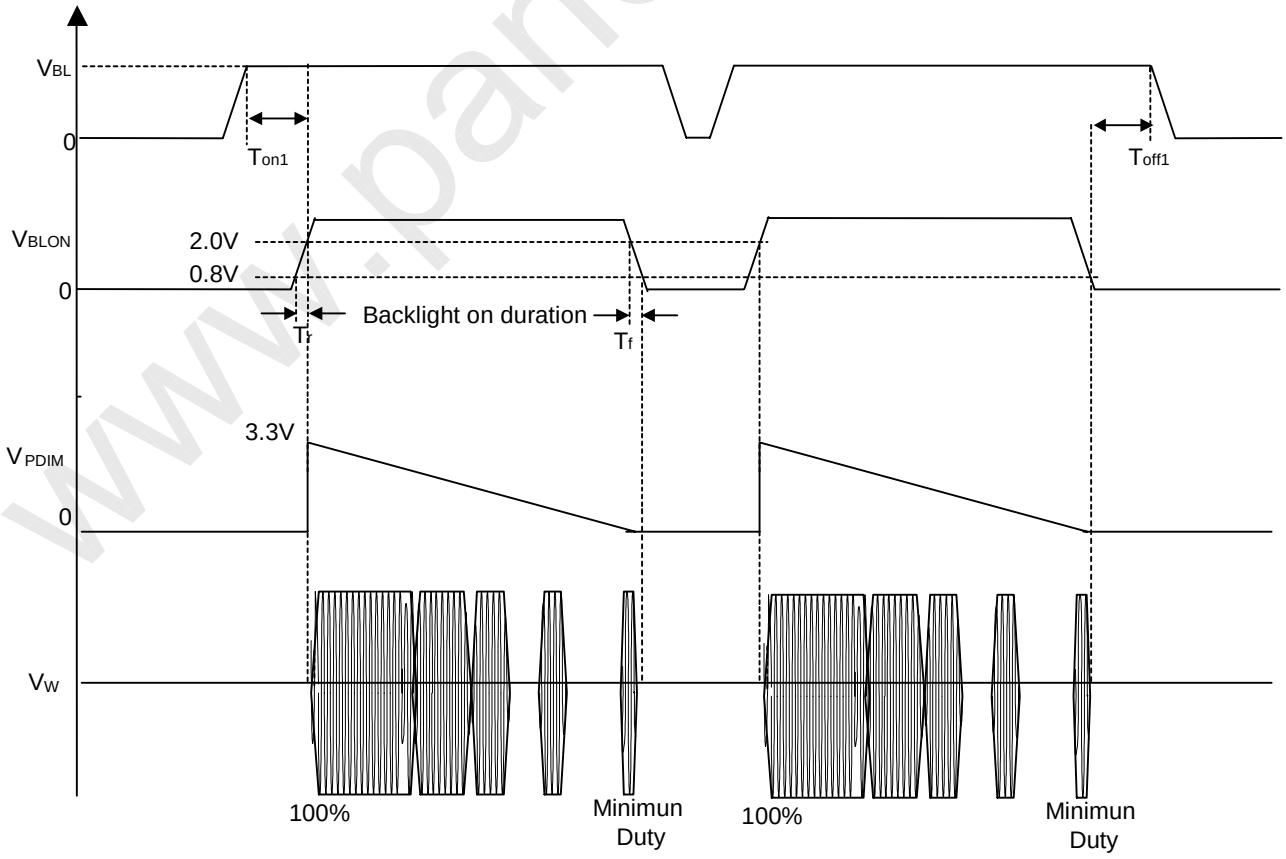
Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 32" backlight unit under input voltage 24V, average lamp current 4.5 mA and lighting 30 minutes later.

3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
ADIM	HI	V_{ADIM}	—	—	—	3.3	V	
	LO		—	—	0	—	V	
PDIM	MAX	V_{PDIM}	V_{SEL} = L	—	—	3.3	V	maximum duty ratio
	MIN			—	0	—	V	minimum duty ratio
Control Signal Rising Time		T_r	—	—	—	100	ms	
Control Signal Falling Time		T_f	—	—	—	100	ms	
ON/OFF Delay Time		T_{on}	—	500	—	—	ms	
ON/OFF Off Time		T_{off}	—	500	—	—	ms	

Note (1) The power sequence and control signal timing are shown as the following figure.



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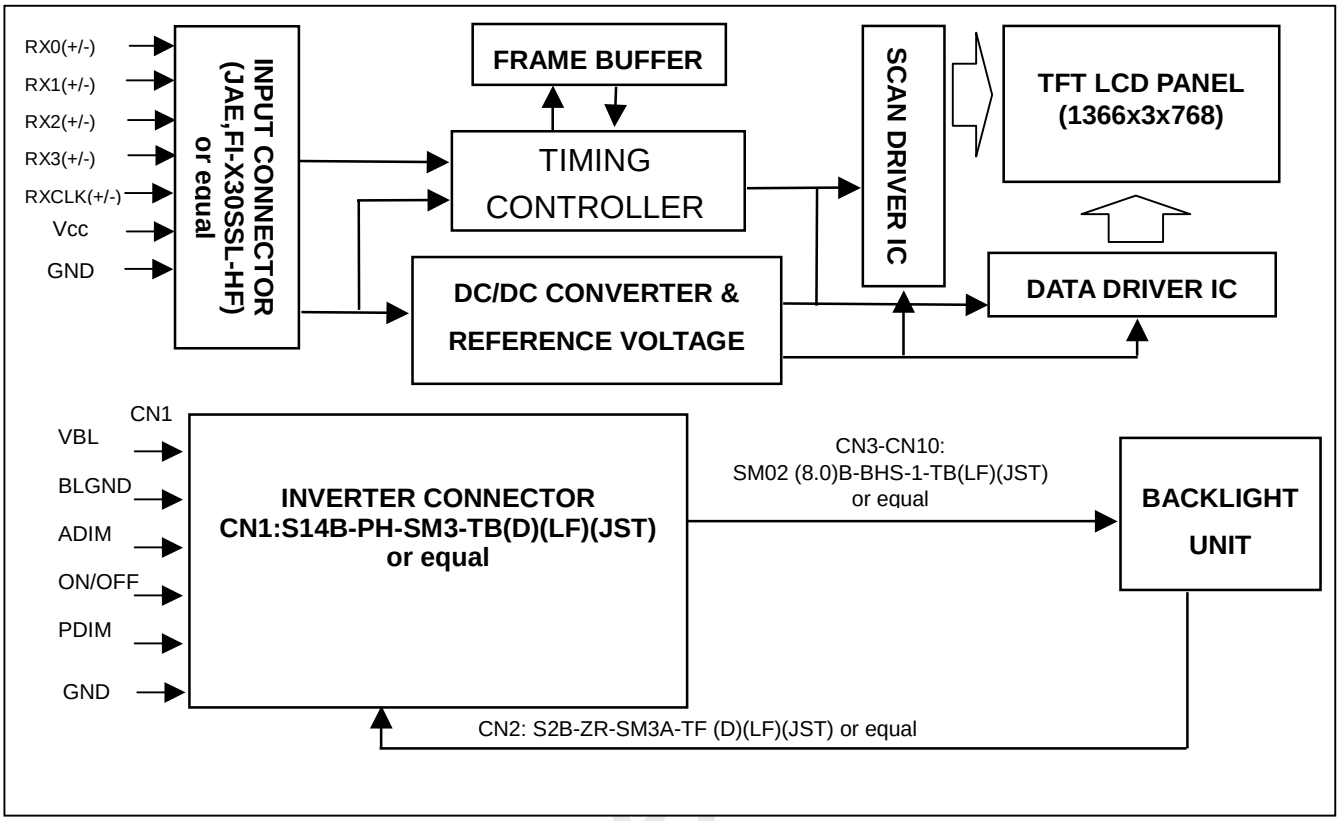
4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



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5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VCC	Power supply: +12V	
2	VCC	Power supply: +12V	
3	VCC	Power supply: +12V	
4	VCC	Power supply: +12V	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	SELLVDS	Select LVDS data format	(2)
10	NC	No Connection	(3)
11	GND	Ground	
12	RX0-	Negative transmission data of pixel 0	
13	RX0+	Positive transmission data of pixel 0	
14	GND	Ground	
15	RX1-	Negative transmission data of pixel 1	
16	RX1+	Positive transmission data of pixel 1	
17	GND	Ground	
18	RX2-	Negative transmission data of pixel 2	
19	RX2+	Positive transmission data of pixel 2	
20	GND	Ground	
21	RXCLK-	Negative of clock	
22	RXCLK+	Positive of clock	
23	GND	Ground	
24	RX3-	Negative transmission data of pixel 3	
25	RX3+	Positive transmission data of pixel 3	
26	GND	Ground	
27	NC	No Connection	(3)
28	NC	No Connection	(3)
29	GND	Ground	
30	GND	Ground	

Note (1) Connector Part No.: FI-X30SSL-HF(JAE) or compatible

Note (2) Please refer to 5.5 LVDS INTERFACE (Page 16)

Note (3) Reserved for internal use. Left it open.

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5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3-CN8 (Housing): BHR-03VS-1(JST) or equivalent

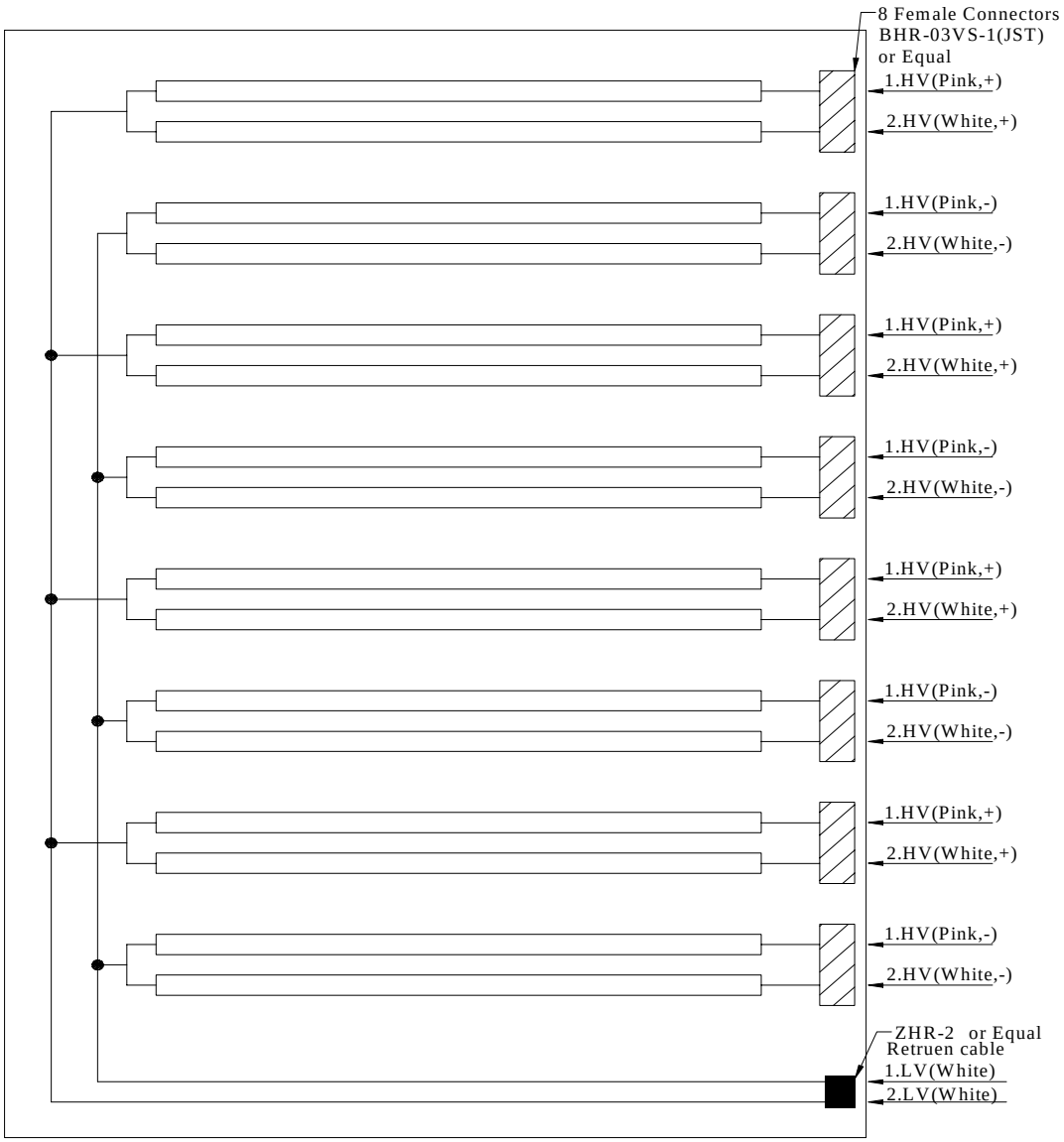
Pin No.	Symbol	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-03VS-1, manufactured by JST or equivalent. The mating header on inverter part number is SM02(8.0)B-BHS-1-TB(LF).

CN9 (Housing): ZHR-2 (JST) or equivalent

Pin No.	Symbol	Description	Wire Color
1	LV	Low Voltage (+)	Black
2	LV	Low Voltage (-)	White

Note (2) The backlight interface housing and return cable for low voltage side is a model ZHR-2 , manufactured by JST or equivalent. The mating header on inverter part number is S2B-ZR-SM3A-TF(D)(LF) or equivalent.



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5.3 INVERTER UNIT

CN1(Header): S14B-PH-SM3-TB(D)(LF)(JST) or equivalent..

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		
11	ADIM	GND (0V) 80% / Open (1.6V) 100% / High (3.3V) 120%, Luminance
12	ON/OFF	BL ON/OFF
13	PDIM	Open/High (3.3V, 100% Duty) for 100%
14	GND	GND

CN2(Header): S2B-ZR-SM3A-TF(D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	CCFL COLD	CCFL low voltage (+)
2	CCFL COLD	CCFL low voltage (-)

CN3-CN8(Header): SM02(8.0)B-BHS-1-TB(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

Note (1) Floating of any control signal is not allowed.

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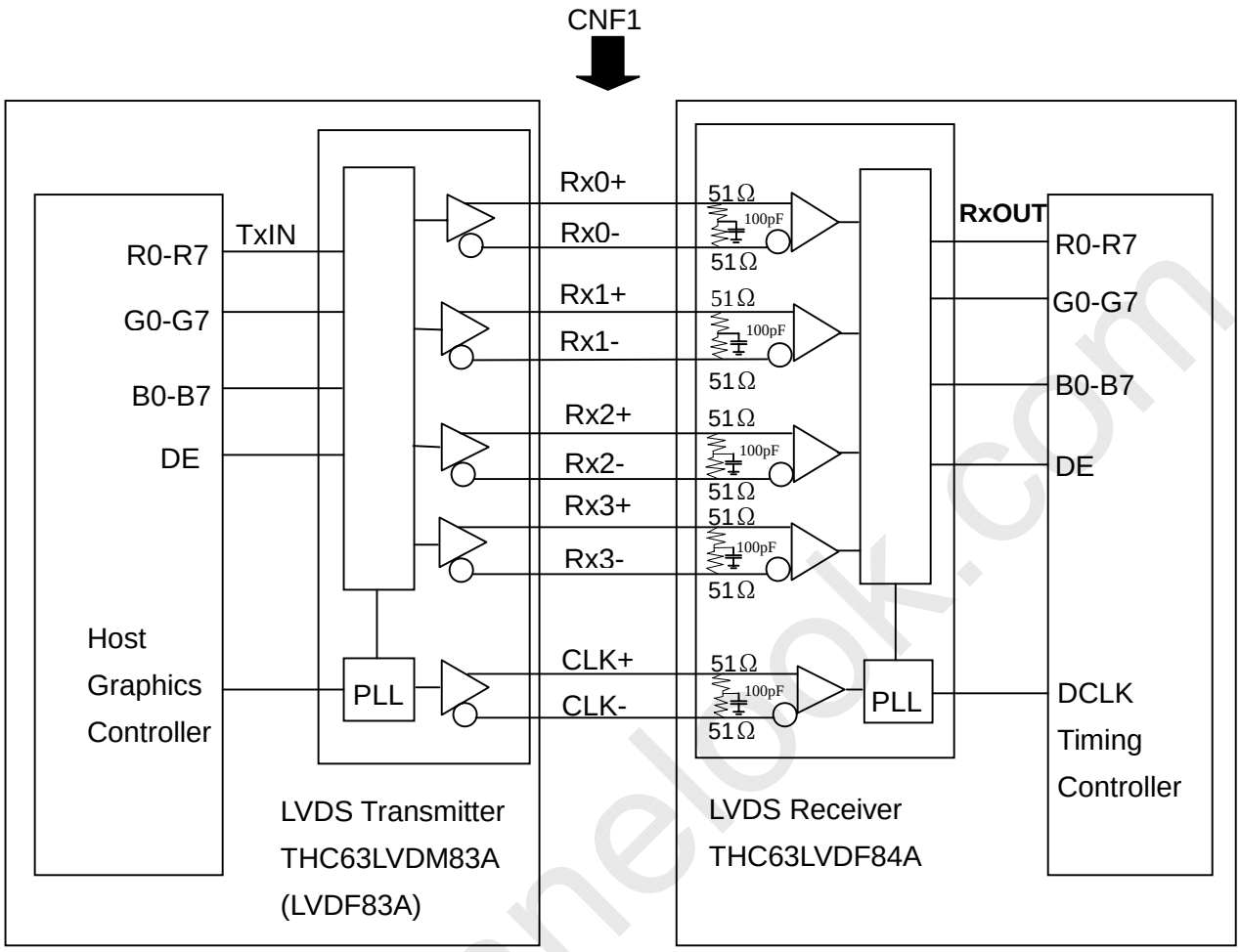
5.4 BLOCK DIAGRAM OF INTERFACE



R0~R7 : Pixel R Data ,
G0~G7 : Pixel G Data ,
B0~B7 : Pixel B Data ,
DE : Data enable signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

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5.5 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	SELLVDS =L or OPEN	SELLVDS =H	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	SELLVDS =L or OPEN	SELLVDS =H
24 bit	R0	R2	51	TxIN0			27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
	DCLK		31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK	

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

Notes(1) RSVD(reserved)pins on the transmitter shall be “H” or(“L” or OPEN)

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5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

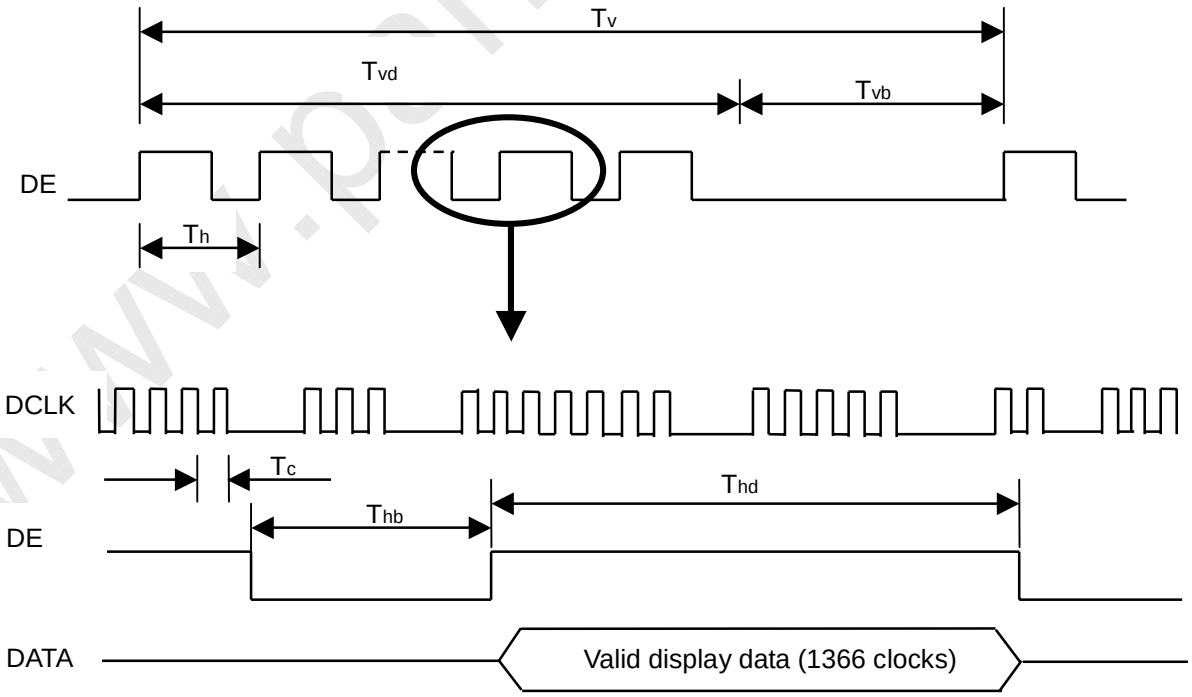
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	86	88	MHz	
	Input cycle to cycle jitter	Trcl	-	-	200	ps	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(2)
		-	57	60	63	Hz	
	Total	Tv	778	795	888	Th	Tv=Tvd+Tvb
	Display	Tvd	768	768	768	Th	-
	Blank	Tvb	10	27	120	Th	-
Horizontal Active Display Term	Total	Th	1442	1798	1936	Tc	Th=Thd+Thb
	Display	Thd	1366	1366	1366	Tc	-
	Blank	Thb	76	432	570	Tc	-

Note (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

(2) Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM



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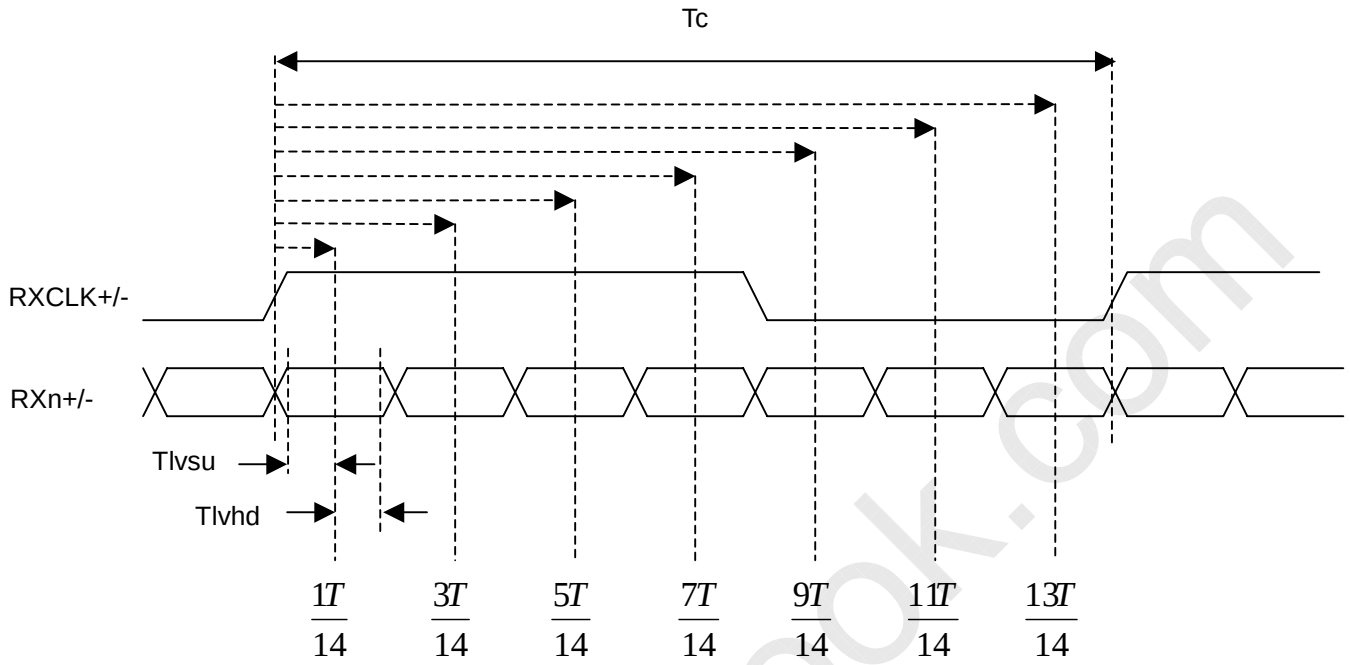
LVDS RECEIVER INTERFACE TIMING DIAGRAM



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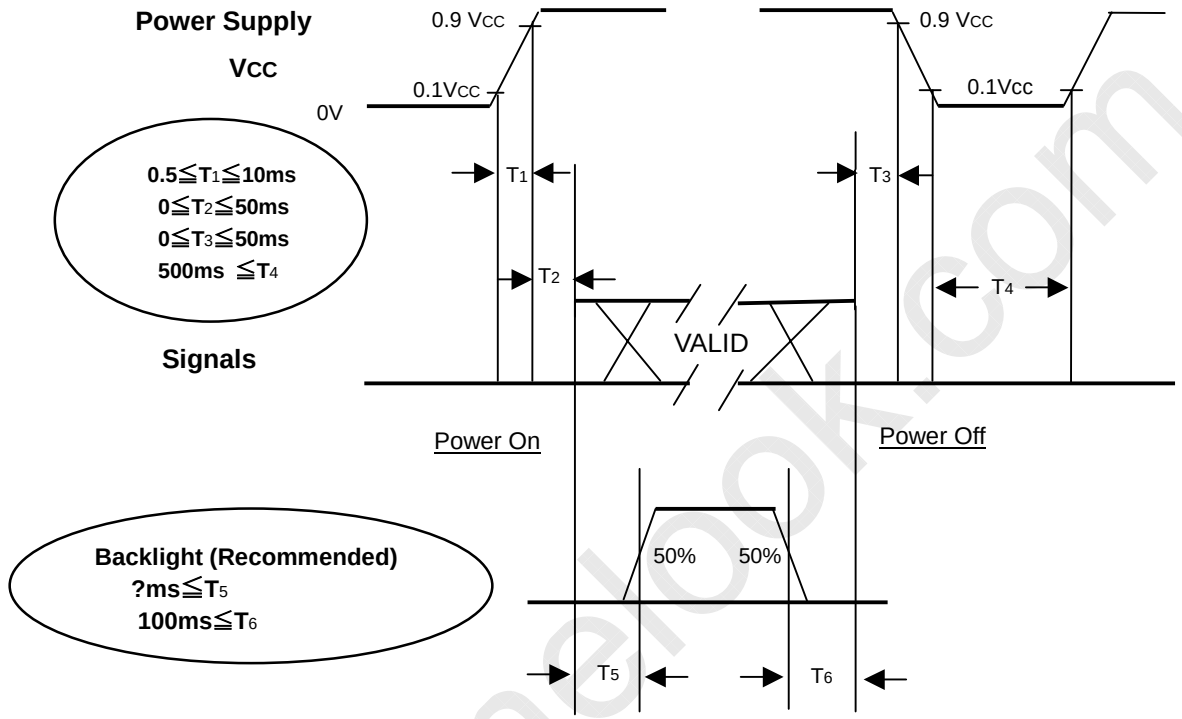
6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

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7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	4.2mA ± 0.5	mA
Oscillating Frequency (Inverter)	F_W	58±3	KHz
Frame rate		60	Hz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	(900)	(1200)	-	-	(2)
Response Time		Gray to gray average		-	(6.5)		ms	(3)
Center Luminance of White		L_C			(500)	-	cd/	(4)
Average Luminance of White		L_{AVE}			(400)	-	cd/	
White Variation		δW		-	-	1.3	-	(7)
Cross Talk		CT		-	-	4.0	%	(5)
Color Chromaticity	Red	Rx			(0.652)		-	(6)
		Ry			(0.331)		-	
	Green	Gx			(0.275)		-	
		Gy			(0.594)		-	
	Blue	Bx			(0.143)		-	
		By			(0.063)		-	
	White	Wx			0.285		-	
		Wy			0.293		-	
	Color Gamut	CG			75		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20		88	-	Deg.	(1)
		θ_x-			88	-		
	Vertical	θ_Y+			88	-		
		θ_Y-			88	-		

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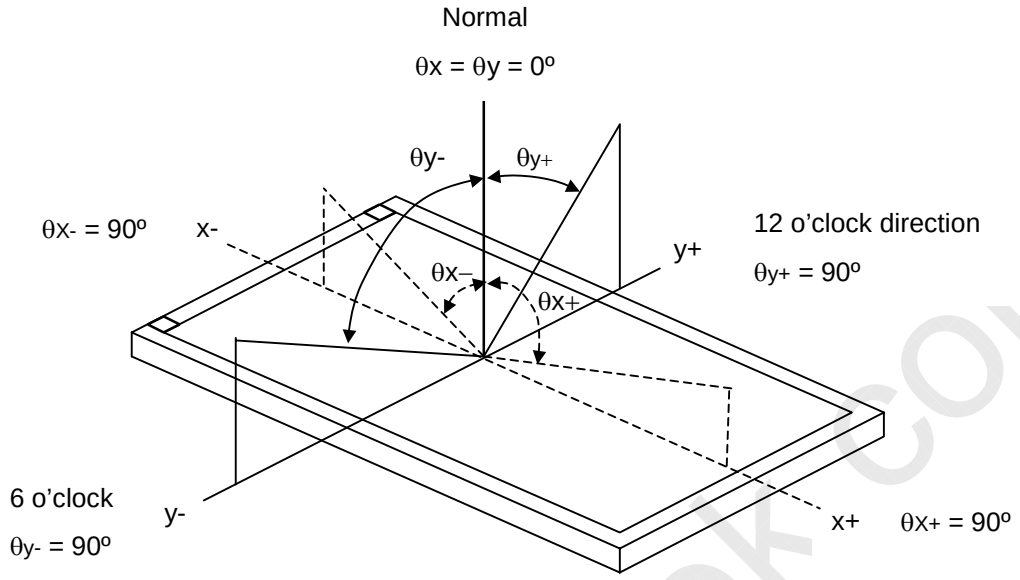
Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

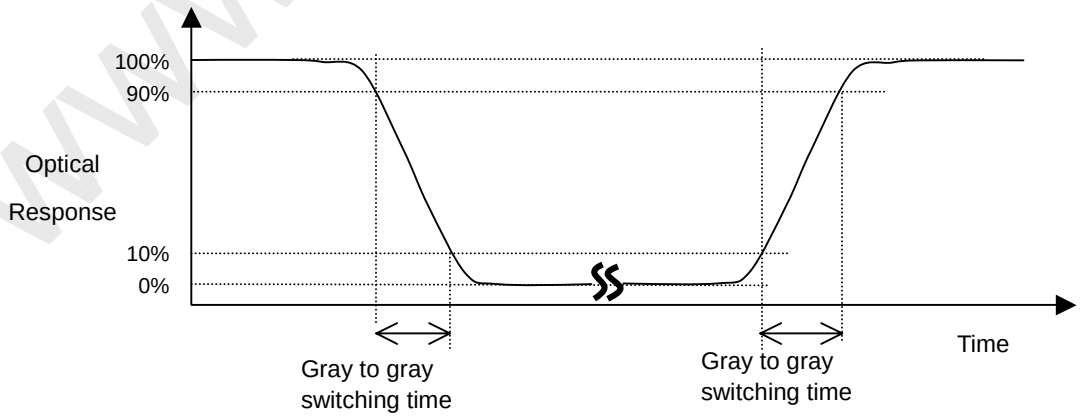
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



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The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other .

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

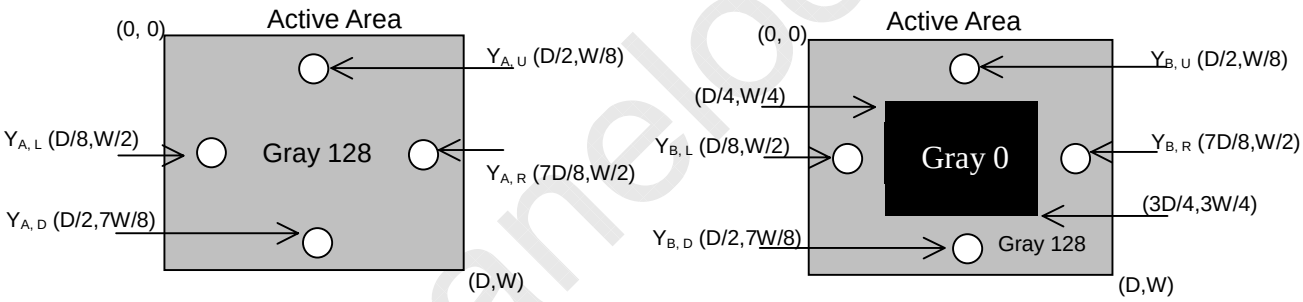
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



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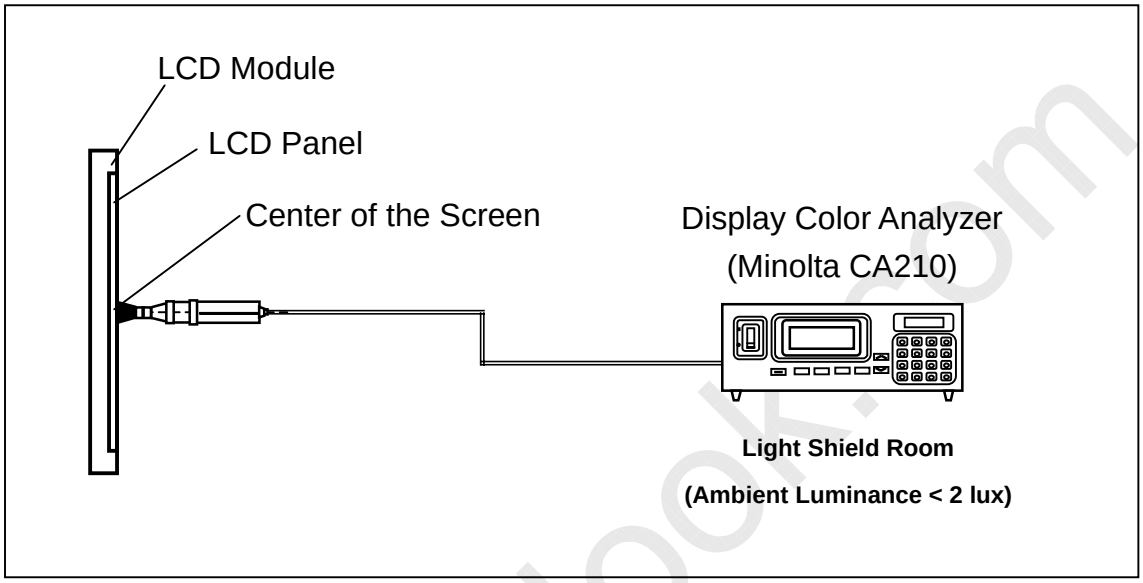
Note (6) Measurement Setup:

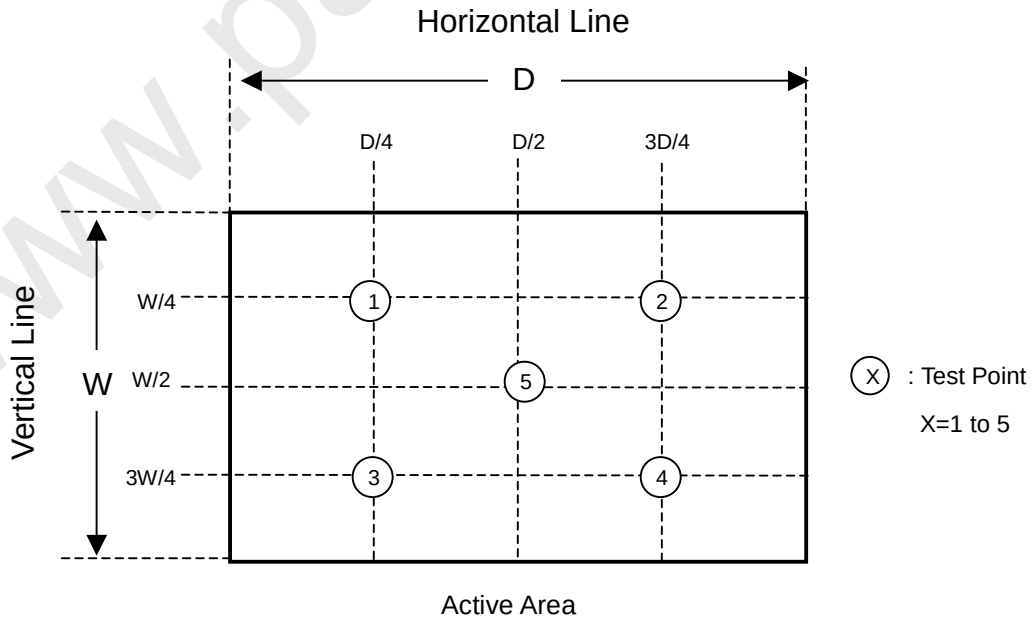
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



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8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

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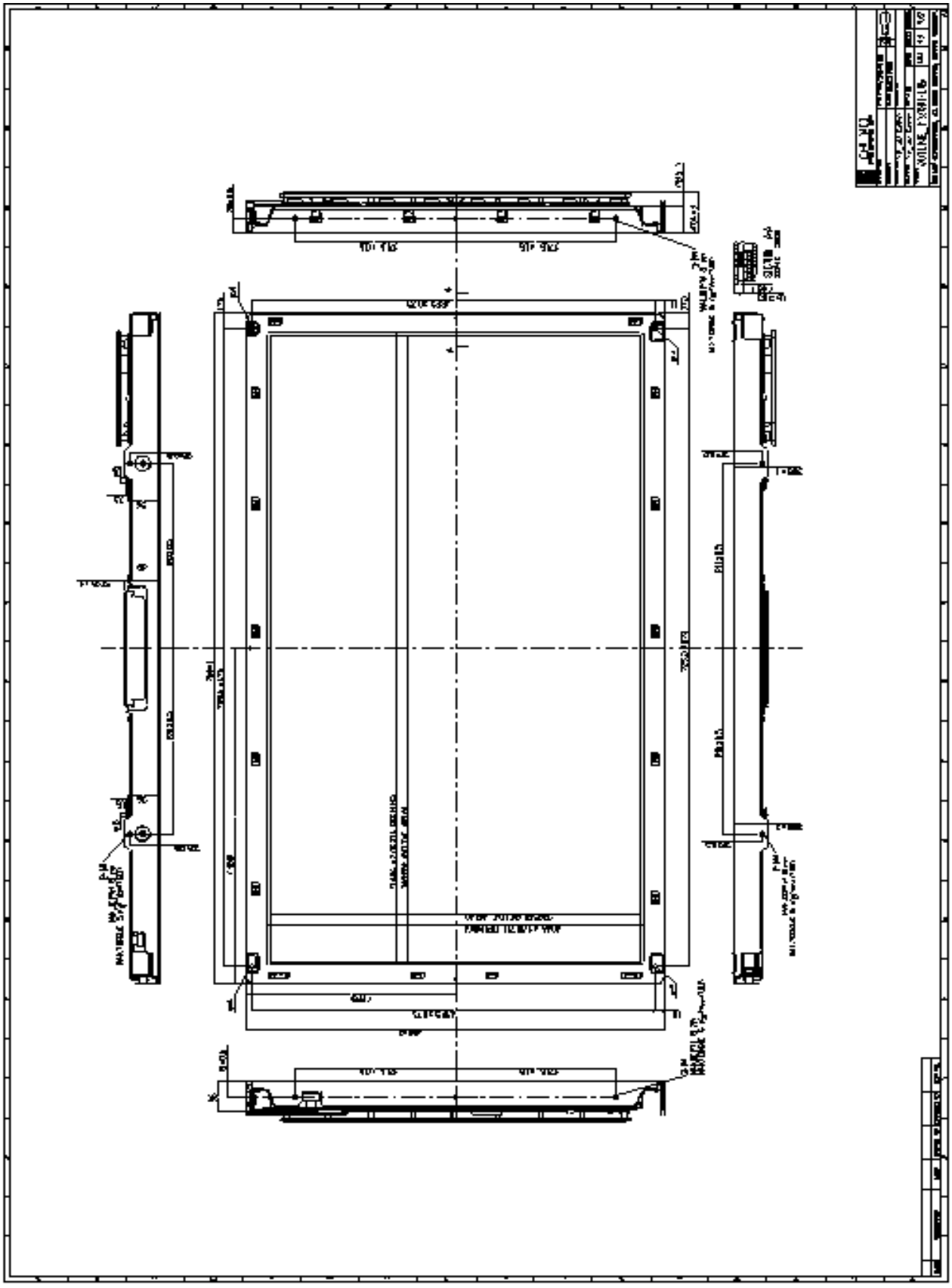
9. MECHANICAL CHARACTERISTICS



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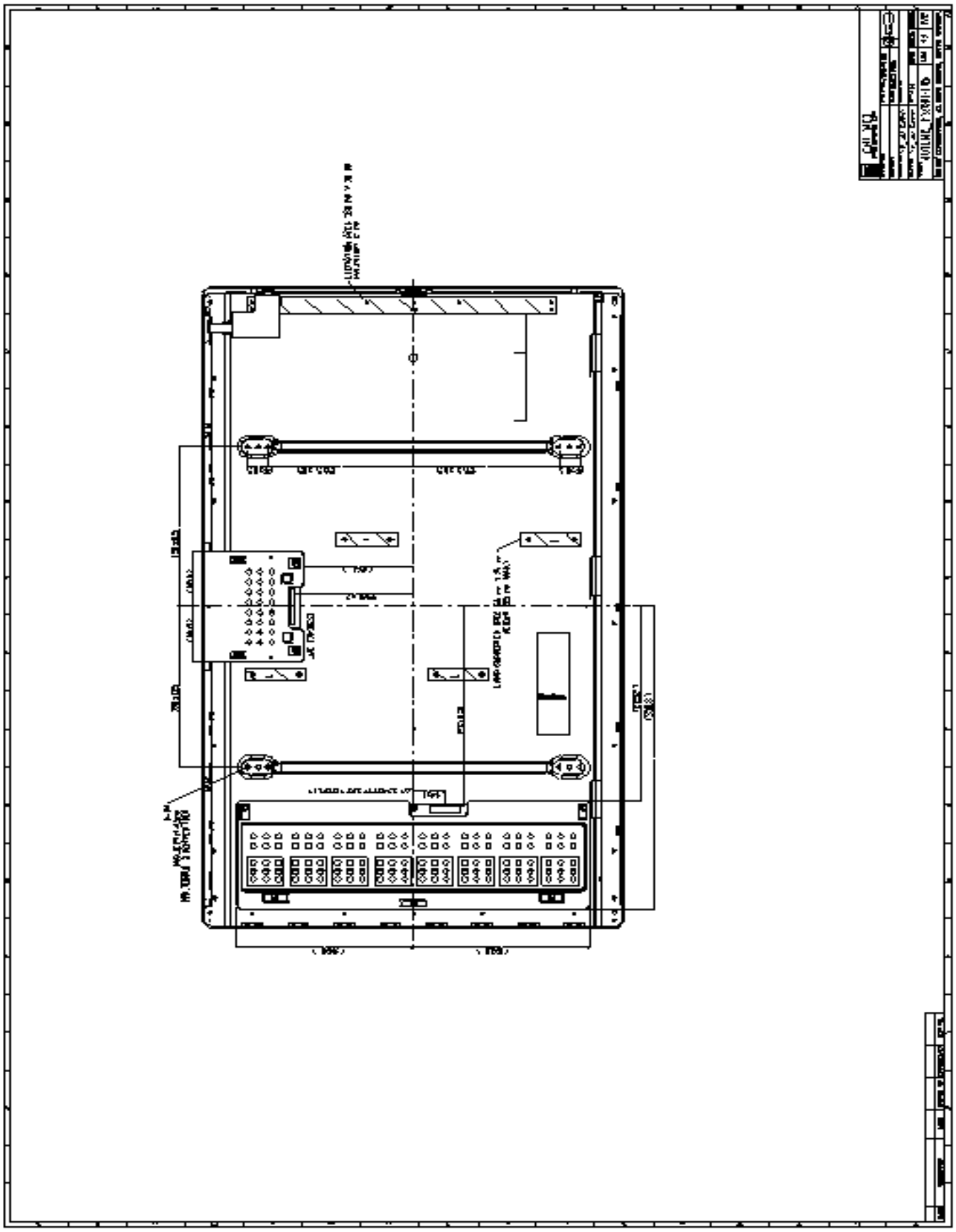

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